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**Dated: May 4, 2006**

Signature:

(Andrew T. Zidel)

Docket No.: SCEI 3.0-178  
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:  
Koji Hirairi

Application No.: 10/801,308

Group Art Unit: 2195

Filed: March 16, 2004

Examiner: M. A. T. An

For: METHODS AND APPARATUS FOR  
REDUCING POWER DISSIPATION IN A  
MULTI-PROCESSOR SYSTEM

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

## INFORMATION DISCLOSURE STATEMENT

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It is respectfully requested that the references listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each non-US reference is enclosed. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material.

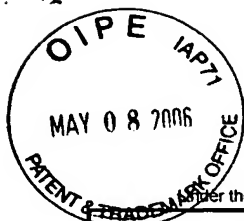
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Dated: May 4, 2006

Respectfully submitted,

By [Signature]  
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PTO/SB/08a/b (07-05)

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				Application Number	10/801,308-Conf. #2000
				Filing Date	March 16, 2004
				First Named Inventor	Koji Hirairi
				Art Unit	2127
				Examiner Name	Not Yet Assigned
Sheet	1	of	1	Attorney Docket Number	SCEI 3.0-178

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
	AA*	US-2002/0053684-A1	05/2002	Chauvel et al.	
	AB*	US-2002/0065049-A1	05/2002	Chauvel et al.	
	AC*	US-2003/0125900-A1	07/2003	Orenstien et al.	
	AD*	US-5,274,797	12/1993	Barlow et al.	
	AE*	US-5,715,184	02/1998	Tyler et al.	
	AF*	US-5,761,516	06/1998	Rostoker et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	CA	Skadron et al., "Temperature-Aware Microarchitecture: Modeling arid Implementation," ACM trans-on architecture and Code optimization, pp. 94-125, March 2004.	
	CB	Azevedo et al., "Architectural and Compiler Strategies for Dynamic Power Management in the COPPER Project," 2001 International Workshop on Innovative Architecture, January, 2001. -	
	CC	Heo et al., "Reducing Power Density through Activity Migration," Proceedings of the 2003 International Symposium on Low Power Electronics and Design (ACM Press, ©2003), pp. 217-222.	
	CD	Tiwari et al. "Instruction Level Power Analysis and Optimization of Software," Journal of VLSI Signal Processing, Vol. 13, No.2 (August 1996), pp. 1-18.	
	CE	Abhishek Mehta, "Techniques for Low Power Processing - A Survey" CSE 822, Spring 2001, A29838087, Retrieved from the Internet on March 29, 2004, cURL: w~w.cs.vcr.edu/~chzhanp/paners read/lowpower survey.pdf>; 10 pages.	-
	CF	Lee et al., "Power Analysis and Minimization Techniques for Embedded DSP Software," IEEE Transactions on VLSI Systems, Vol. 5, No. 1, March 1997, pp. 123-135 (manuscript copy submitted).	
	CG	Gerosa et al., "A 250-MHz 5-W PowerPC Microprocessor with On-Chip 1.2 Cache Controller," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1635-1649.	-

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